REMARKS

Claims 1-19 are pending in the present application, were examined, and stand rejected. In response, Applicants amend Claim 18. Applicants respectfully request reconsideration of pending Claims 1-19, as amended, and in view of at least the following remarks.

I. CLAIM OBJECTION

Claim 18 has been amended to address the informalities cited by the Examiner in the Office Action.

II. CLAIMS REJECTED UNDER 35 U.S.C. §102

The Patent Office rejected Claims 1-4, 6, 8, 10-16 and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,884,057 issued to Blomgren, et al. ("Blomgren"). Applicants respectfully traverse this rejection.

Applicants respectfully assert that the Examiner has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(e). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Claim 1 includes the following features which are neither taught nor suggested by either Blomgren or the references of record. Specifically, Claim 1 requires:

> a first instruction set engine to process instructions from a first ISA having a first ISA word size;
>
> a second instruction set engine to process instructions from a second ISA having a second ISA word size, the first ISA word size being larger than the second ISA word size. [Emphasis added]

However, according to the Examiner, Blomgren teaches first and second instructions set engines to process instructions having a first word size and a second word size, the second word size being difference (sic) than the first word size. (Col. 6, lines 40-42) However, after having carefully reviewed the relevant portions of Blomgren cited by the Examiner, Applicants must respectfully disagree with the Examiner's contention.

Applicants submit that the teachings of Blomgren are limited to processing opcodes of different lengths. Applicants submit that there is no suggestion as to any variation in the word sizes between the RISC and CISC instruction sets within Blomgren.

Specifically, the Examiner's attention is drawn to the following quote from Blomgren:

> The RISC and CISC instruction sets have independent encoding of instructions to opcodes. While both sets have ADD operations, the opcode number which encodes the ADD operation is different for the two instruction sets. In fact, the size and location of the opcode field in the instruction word is also different for the two instruction sets. Thus two instruction decoders are used for the two instruction sets – a RISC decoder 36 and a CISC decoder 32. (Col. 6, lines 37-44) [Emphasis added]

As indicated, CISC instruction sets and RISC instruction sets use independent encoding of instructions into opcodes. In addition, the size and location of the opcode field in **the** instruction word is different for the two instruction sets. Applicants submit that the cited passage implies that the instruction word size is the same for both the CISC and RISC instruction sets. Unless the CISC and RISC instruction words are the same size, Blomgren's indication of "the size and location of the opcode field in **the** instruction word being different for the two instruction sets" makes no sense. Use of the definite article in this context requires a single instruction word size. Accordingly, one skilled in the art would not interpret Blomgren as teaching instruction set engines for processing instructions from ISAs having different word sizes.

Moreover, after carefully reviewing the entire text of Blomgren, Applicants respectfully submit that the Examiner's characterization of Blomgren is incorrect. Blomgren teaches a mechanism for rapid reconfiguration of pipeline alignment between a pipeline optimized for RISC instructions and one optimized for CISC instructions with the use of muxes and mode registers. (Abstract, and also as depicted with reference to Blomgren's Fig. 2)

Furthermore, as known to those skilled in the art, CISC instructions use memory operands, while RISC instructions use only register operands. (Col. 1, lines 47-51) Thus,

> for RISC operations the pipeline is most efficient when memory access stages of the pipeline are located late in the pipeline, such as in the execute stage. However, for CISC operations the memory access stages must be located early in the pipeline before the execute stage so they can deliver a memory operand to the execute stage. (Col. 1, lines 50-55)

To this end, Blomgren describes various mechanisms for aligning the CISC and RISC pipelines, as depicted with reference to Figs. 2-3 and 5-7. Applicants submit that the entire description of Blomgren is devoid of any reference to providing processing for different ISAs having different ISA word sizes. However, the case law is quite clear in establishing that each and every element of the claim must be exactly disclosed in the anticipatory reference. Banner Titanium, *Id.*

Furthermore, Claim 1 requires the following feature, which is neither taught nor suggested by either Blomgren or the references of record:

a floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output.

Applicants respectfully submit that Blomgren fails to teach the processing of an input responsive to a mode identifier. Specifically, Blomgren teaches:

> Switching between RISC and CISC modes is under the control of pipeline and mode control logic 30. Mode logic 30 sets or clears the RISC/CISC bit 60 mode register 38 to reconfigure the pipeline alignment using mux 26. In addition, mode bit 60 enables the output from one of the two instruction decoders using mux 46. (Col. 6, lines 56-61.)

As illustrated with reference to FIG. 4 of Blomgren, mux 46 selects a decoded instruction from risk instruction decoder 36 when a risk mode is indicated by mode register 38. Conversely, mux 46 selects a decoded instruction from CIS instruction decoder 32 when mode register 38 indicates a CISC mode. (*See* col. 3, lines 2-9.) In other words, Applicants respectfully submit that Blomgren teaches the selection of decoded instructions from one of a CISC instruction set architecture or an RISC instruction set architecture, depending on a mode indicated by a mode register. Conversely, Claim 1 requires processing of a data input responsive to the mode identifier. As such, Applicants submit that this feature is neither taught nor suggested by either Blomgren or the references of record.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 1 under 35 U.S.C. §102(e) in view of Blomgren. Therefore, Applicants respectfully submit that Claim 1 is patentable over Blomgren, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 1.

CLAIMS 2-4 and 6-9:

Regarding Claims 2-4 and 6-9, Applicants respectfully submit that Claims 2-4 and 6-9 depend from Claim 1 and therefore include the patentable claim features of Claim 1. Accordingly, for at least the reasons described above, Claims 2-4 and 6-9 are patentable over Blomgren, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 2-4, 6 and 8.

CLAIM 10:

Regarding Claim 10, Claim 10 includes the following features, which are neither taught nor suggested by either Blomgren or the references of record:

> fetching an input from at least one of a plurality of floating-point registers;
>
> if the token is detected in the input, checking what mode the processor is in;
>
> if the processor is in a first mode, processing the input to render an arithmetic result operation;
>
> if the processor is in a second mode, performing a token specific operation

Applicants submit that these features are neither taught nor suggested by either Blomgren or the references of record.

The Examiner directs Applicants to col. 6, lines 64-65 wherein,

> the CISC instruction decoder 32 detects these emulated instructions and signals from unknown opcode over line 40 to mode control logic 30. In response, the mode control logic 30 sets RISC bit-60 in register 38 and loads the instruction pointer with the address of the emulation routine in memory. Once the emulation routine is complete, an RISC instruction causes the mode register 38 to be reset to CISC mode and the instruction pointer updated to point to the following CISC instruction. The CISC program continues with the following instruction unaware that the instruction was emulated with RISC instructions. (See cols. 6-7 lines 61-10) [Emphasis added]

As is clearly indicated by the cited passage, there is no reference to whether a check of whether a token is received as a data input, as required by Claim 10. However, the case law is quite clear that each and every element of the claim must be exactly disclosed in the anticipatory reference. Banner Titanium, *Id.*

Accordingly, although Blomgren describes emulation of certain CISC routines with RISC instructions, the processing performed within Blomgren does not vary according to the mode bit. As indicated above, the mode bit directs mux 46 to select either a decoded CISC instruction or a decoded RISC instruction. Furthermore, the detection of emulated instructions does not teach the detection of a token as a data input operand, as required by Claim 10.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 10 under 35 U.S.C. §102(e) in view of Blomgren or the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 10.

CLAIMS 11-16:

Claims 11-16 depend from Claim 10 and, therefore, include the patentable claim limitations of Claim 10, as described above. Accordingly, Applications respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 11-16.

CLAIM 19:

Regarding Claim 19, Claim 19 includes similar features to Claim 10, which is neither nor suggested by the references of record. Furthermore, Claim 19 includes the following features, which are neither taught nor suggested by either Blomgren or the references of record:

> processing the input to render an arithmetic result when the processor is in at least a first mode of a plurality of modes; and
>
> performing a token specific operation when the processor is in at least a second mode of a plurality of modes.

As indicated above, Blomgren teaches the emulation of complex CISC instructions using a plurality of RISC instructions, which are referred to as "emulated instructions".

> The instruction decoder 32 is responsible for detecting such instructions, which results in the setting of an RISC mode and loading of the emulation routine in memory, such that following execution, the mode register 38 is reset to CISC mode and the instruction pointer is updated to point to the following CISC instruction. (Col. 7, lines 1-10.)

In contrast, Claim 19, as amended, requires detection of whether a token is received as an input operand of an operation. If a token is received, the token may be processed to produce an arithmetic result when the processor is in a first mode. However, if the processor is in a second mode, a token specific operation is performed by the processor. As such, Claim 19 requires varied operation, depending on whether a token is received as an input operand corresponding to a received operation.

Conversely, Blomgren teaches the detection of an emulated CISC instruction and switches modes when such an instruction is detected to a RISC mode, resulting in the loading of various RISC instructions to perform the CISC instruction, which once completed, returns the mode to the CISC mode. Applicants respectfully submit that the instruction emulation as taught by Blomgren does not provide any teachings or suggestions with reference to processing of tokens received as data input operands when in a first mode and processing a token specific operation when the processor is in a second mode, as required by Claim 19, as amended.

Consequently, Applicants submit that the Examiner has failed to establish a *prima facie* rejection of Claim 19 under 35 U.S.C. §102(e) since Blomgren fails to teach each and every element of Claim 19, as amended. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 19.

III. CLAIMS REJECTED UNDER 35 U.S.C. §103

CLAIM 5:

The Patent Office rejected Claim 5 under 35 U.S.C. §103(a) as being unpatentable over Blomgren in view of U.S. Patent No. 5,884,057 issued to Dao et al. ("Dao"). Applicants respectfully traverse this rejection.

Applicants submit that Claim 5 depends from Claim 1 and therefore indicates the patentable claim features of Claim 1, as described above. Furthermore, Applicants submit that the Examiner's combination in view of Dao fails to rectify the deficiencies attributed in Blomgren for failing to teach or suggest a processor for processing instructions from first and second ISAs where the first ISA word size is different than the second word size.

Consequently, for at least the reasons described above, Claim 5 is patentable over the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 5.

CLAIMS 7, 9 and 17:

The Patent Office rejected Claims 7, 9 and 17 under 35 U.S.C. §103(a) as being unpatentable over Blomgren in view of IEEE Standard for Binary Floating-Point Arithmetic ("IEEE"). Applicants respectfully traverse this rejection.

Applicants submit that Claims 7 and 9 dependent from Claim 1 and therefore include the patentable claim features of Claim 1. Furthermore, with regards to the citing of IEEE reference, Applicants submit that the IEEE reference fails to rectify the deficiencies attributed to Blomgren and failing to teach processing of first and second ISAs where the first ISA word size is different than the second ISA word size.

Accordingly, for at least the reasons described above, Claims 7 and 9 are patentable over Blomgren and IEEE, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 7 and 9.

Regarding Claim 17, Claim 17 depends from Claim 10 and therefore includes the patentable claim features of Claim 10, as described above. With regard to the IEEE reference, the IEEE reference fails to rectify the deficiencies attributed to Blomgren's failure to teach detection of a token as a data input operand of a received operation, as well as the processing of the token operand based on the indicated mode.

Accordingly, for at least the reasons described above, Claim 17 is patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 17.

CLAIM 18:

The Patent Office rejected Claim 18 under 35 U.S.C. §103(a) as being unpatentable over Blomgren in view of U.S. Patent No. 5,204,828 issued to Kohn ("Kohn"). Applicants respectfully traverse this rejection.

Applicants respectfully submit that Claim 18, as amended, includes the following claims features, which are neither taught nor suggested by either Blomgren in view of Kohn, as well as the references of record:

> a plurality of instruction set engines to process instructions from a plurality of instruction set architectures having different word sizes.

Applicants submit that this feature is neither taught nor suggested by either Blomgren or Kohn. As indicated above, Blomgren's teachings are limited to processing of RISC instruction set architectures, as well as CISC instruction set architectures. Although the Examiner indicates that CISC instruction sets may have varying word sizes, an architecture generally is limited to a maximum word size, as indicated by the 32-bit size provided within the RISC ISAs.

In contrast, Claim 18 requires instruction set engines for processing instruction from ISAs having different word sizes. Such a teaching or suggestion is found in neither Blomgren nor Kohn.

To wit, Applicants submit that the passage cited by the Examiner (*See* col. 16, lines 37-44) implies that the instruction word size is the same for both the CISC and RISC instruction sets. Unless the CISC and RISC instruction words are the same size, Blomgren's indication of "the size and location of the opcode field in the instruction word being different for the two instruction sets" makes no sense. Accordingly, one skilled in the art would not interpret Blomgren as teaching instruction set engines for processing instructions from ISAs having different word sizes.

Furthermore, Claim 18, as amended, requires the processing of an input responsive to a mode identifier. In contrast, Blomgren teaches the selection of a decoded instruction from either a RISC instruction decoder or a CISC instruction decoder, depending on an indicated mode. There is no teachings or suggestions to processing an input, depending on the mode indicated.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness over Blomgren in view of Kohn in order to reject Claim 18. Claim 18, as amended, includes several patentable claim features, which are neither taught nor suggested by either Blomgren or Kohn. Consequently, Claim 18, as amended, is patentable over the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 18.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-19, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: Aug. 12, 2003

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail , with sufficient postage, in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 08-12, 2003

Marilyn Bass

Marilyn Bass Aug. 12, 2003